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Dated: June 22, 2004

Signature: 
(Andrew T. Zidel)

Docket No.: SCEI 3.0-200
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Keisuke Inoue

Application No.: 10/812,155

Group Art Unit: 2115

Filed: March 29, 2004

Examiner: Not Yet Assigned

For: METHODS AND APPARATUS FOR
ACHIEVING THERMAL MANAGEMENT
USING PROCESSOR MANIPULATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. §1.97(b)

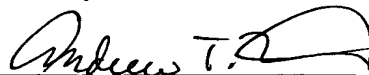
Dear Sir:

It is respectfully requested that the references listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. In accordance with the notice at 1276 O.G. 55, copies of U.S. patent and patent application references are not enclosed herewith; copies of non-U.S. patent references are submitted herewith. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material.

In the event that any fee is due in connection with the present Information Disclosure Statement, the Commissioner is hereby authorized to charge the same to our Deposit Account No. 12-1095.

Dated: June 22, 2004

Respectfully submitted,

By 
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LD-458\



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Substitute for form 1449A/B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			Application Number	10/812,155	
			Filing Date	3/29/2004	
			First Named Inventor	Keisuke Inoue	
			Art Unit	2115	
			Examiner Name	Not Yet Assigned	
Sheet	1	of	1	Attorney Docket Number	SCEI 3.0-200

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US-5,274,797	12/28/1993	Barlow et al.	
	AB	US-5,715,184	02/03/1998	Tyler et al.	
	AC	US-5,761,516	06/02/1998	Rostoker et al.	
	AD	US-2002/0053684 A1	05/09/2002	Chauvel et al.	
	AE	US-2002/0065049 A1	05/30/2002	Chauvel et al.	
	AF	US-2003/0125900 A1	07/03/2003	Orenstien et al.	

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					

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NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
	CA	Azevedo et al., "Architectural and Compiler Strategies for Dynamic Power Management in the COPPER Project," 2001 International Workshop on Innovative Architecture, January 2001.		
	CB	Heo et al., "Reducing Power Density through Activity Migration," Proceedings of the 2003 International Symposium on Low Power Electronics and Design (ACM Press, ©2003), pp. 217-222.		
	CC	Tiwari et al., "Instruction Level Power Analysis and Optimization of Software," Journal of VLSI Signal Processing, Vol. 13, No. 2 (August 1996), pp. 1-18.		
	CD	Abhishek Mehta, "Techniques for Low Power Processing - A Survey" CSE 822, Spring 2001, A29838087, Retrieved from the Internet on March 29, 2004, <URL: www.cs.vcr.edu/~chzhang/papers_read/lowpower_survey.pdf >; 10 pages.		
	CE	Lee et al., "Power Analysis and Minimization Techniques for Embedded DSP Software," IEEE Transactions on VLSI Systems, Vol. 5, No. 1, March 1997, pp. 123-135 (manuscript copy submitted).		
	CF	Gerosa et al., "A 250-MHz 5-W PowerPC Microprocessor with On-Chip L2 Cache Controller," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1635-1649.		

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Examiner Signature		Date Considered	
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